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EXAMINER	
VUONG, JASON DUY ANH	
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2626	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,185	ITOH, NAOTSUQU	
	Examiner	Art Unit	
	Jason D. A. Vuong	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 July 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: it is missing.

The applicant is required to submit an oath or declaration in accordance with either 37 CFR 1.66 or 1.68.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "An Image Processing Method And Apparatus Capable Of Rotating and Reversing An Input Image."

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1, 4, 7, 8, 9, 10, 11, 12, and 13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding **Claims 1, 4, 7, 8, 9, 10, 11, 12, and 13**, these claims are considered indefinite because they contain the phrase "rotation/reversal." It is unclear whether the phrase "rotation/reversal" refers to "rotation and reversal," or "rotation or reversal."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1, 2, 3, 4, 5, 6, 7, 8, 11, and 12** are rejected under 35 U.S.C. 102(b) as being anticipated by Kajihara.

Regarding **Claim 1**, an image processing method comprising:

a numerical signal generation step of sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal (Kajihara's method of synchronizing the sequential image data with a pulse is equivalent to having binary signals synchronized with a clock signal. Refer to Column 2 Lines 66-68, and Column 3 Lines 1-3);

a bit exchange step of generating and outputting, from the output signal in said numerical signal generation step being managed as an input signals, a

signal that order of bits in the input signal has been exchanged or a signal that the bits in the input signal have been reversed (Kajihara discloses a bit-order reversing circuit that performs this function. Refer to Figure 3 Elements 11 and 12, and Figure 3 Elements 13 and 14); and

a control step of controlling the bit order exchange operation or the bit reversal operation in said bit exchange step (the controller is controlling the bit-reversing circuit and the rotation circuit. Refer to Figure 3 Element 18),

wherein image data divided into pixel data and one-dimensionally arranged and stored in a memory is read and output in synchronism with the sequential operation in said numerical signal generation step (refer to Column 1 Lines 67-68), and the output signal generated in said bit exchange step is read and output as an address signal (refer to Column 2 Lines 26-27), so that a rotation/reversal process to a former image is performed.

Regarding **Claim 2**, a method according to Claim 1, wherein an input two-dimensional image is represented by an aggregate of the pixel data, and all the pixel data are one-dimensionally arranged and transferred to the memory in synchronism with a clock signal (it is inherent that input images are two-dimensional, and that the sequentially transferred image data is one-dimensional).

Regarding **Claims 3 and 6**, a method according to Claim 1, wherein, in said bit exchange steps plural kinds of bit exchanges can be performed, and one

of the plural kinds of bit exchanges is selected and output according to an angle of rotation or a kind of reversal (Kajihara discloses many ways of performing image rotation. The 0-degree rotation is performed by not reversing the data bits. Refer to Column 5 Lines 52-68, Column 6 Lines 1-4, and Column 7 Lines 34-43. The 90-degree rotation is performed by reversing the data bits and also subjected to further manipulation. Refer to Column 6 Lines 5-55, Column 7 Lines 44-68, and Column 8 Lines 1-13. The 180-degree rotation is described in Column 6 Lines 56-68, Column 7 Lines 1-2, and Column 8 Lines 14-29. The 270-degree rotation is described in Column 6 Lines 3-33, Column 8 Lines 30-46).

Regarding **Claim 4**, an image processing apparatus comprising:

numerical signal generation means for sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal (Kajihara's method of synchronizing the sequential image data with a pulse is equivalent to having binary signals synchronized with a clock signal. Refer to Column 2 Lines 66-68, and Column 3 Lines 1-3);

bit exchange means for generating and outputting, from the output signal of said numerical signal generation means being managed as an input signal, a signal that order of bits in the input signal has been exchanged or a signal that the bits in the input signal have been reversed (Kajihara discloses a bit-order reversing circuit that performs this function. Refer to Figure 3 Elements 11 and 12, and Figure 3 Elements 13 and 14);

control means for controlling the bit order exchange operation or the bit reversal operation of said bit exchange means (the controller is controlling the bit-reversing circuit and the rotation circuit. Refer to Figure 3 Element 18); and

storage means for storing image data (Column 4 Lines 4-7),

wherein the image data divided into pixel data and one-dimensionally arranged and stored in said storage means is read and output in synchronism with the sequential operation of said numerical signal generation means (refer to Column 1 Lines 67-68), and the output signal generated by said bit exchange means is read and output as an address signal (refer to Column 2 Lines 26-27), so that a rotation/reversal process to a former image is performed.

Regarding **Claim 5**, an apparatus according to Claim 4, wherein an input two-dimensional image is represented by an aggregate of the pixel data, and all the pixel data are one-dimensionally arranged and transferred to said storage means in synchronism with the clock signal (it is inherent that input images are two-dimensional, and that the sequentially transferred image data is one-dimensional).

Regarding **Claim 7**, an image processing method comprising:

a numerical signal generation step of sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal (Kajihara's method of synchronizing the sequential image data with a pulse is

equivalent to having binary signals synchronized with a clock signal. Refer to Column 2 Lines 66-68, and Column 3 Lines 1-3);

a bit exchange step of generating and outputting, from the output signal in said numerical signal generation step being managed as an input signal, a signal that order of bits in the input signal has been exchanged or a signal that the bits in the input signal have been reversed (Kajihara discloses a bit-order reversing circuit that performs this function. Refer to Figure 3 Elements 11 and 12, and Figure 3 Elements 13 and 14); and

a control step of controlling the bit order exchange operation or the bit reversal operation in said bit exchange step (the controller is controlling the bit-reversing circuit and the rotation circuit. Refer to Figure 3 Element 18),

wherein image data is written in a memory in synchronism with the sequential operation in said numerical signal generation step and by using the output signal generated in said bit exchange step as an address signal, and the image data written in the memory is read according to addresses of predetermined order (for the case of 0-degree rotation, data address is read out in a particular way. Refer to Column 6 Lines 2-4. Lines 50-54 of Column 6 describe the address reading for the case of 90-degree rotation. Lines 60-63 of Column 6 describe the address reading for the case of 180-degree rotation. Lines 9-15 of Column 7 describe the address reading for the case of 270-degree rotation), so that a rotation/reversal process to a former image is performed.

Regarding **Claim 8**, an image processing apparatus comprising:

numerical signal generation means for sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal (Kajihara's method of synchronizing the sequential image data with a pulse is equivalent to having binary signals synchronized with a clock signal. Refer to Column 2 Lines 66-68, and Column 3 Lines 1-3);

bit exchange means for generating and outputting from the output signal of said numerical signal generation means being managed as an input signal, a signal that order of bits in the input signal has been exchanged or a signal that the bits in the input signal have been reversed (Kajihara discloses a bit-order reversing circuit that performs this function. Refer to Figure 3 Elements 11 and 12, and Figure 3 Elements 13 and 14);

control means for controlling the bit order exchange operation or the bit reversal operation of said bit exchange means (the controller is controlling the bit-reversing circuit and the rotation circuit. Refer to Figure 3 Element 18); and

storage means for storing image data (Column 4 Lines 4-7),

wherein the image data is written in said storage means in synchronism with the sequential operation of said numerical signal generation means and by using the output signal generated by said bit exchange means as an address signal, and the image data written in said storage means is read according to addresses of predetermined order, so that a rotation/reversal process to a former image is performed (for the case of 0-degree rotation, data address is read out in a particular way. Refer to Column 6 Lines 2-4. Lines 50-54 of Column 6 describe the address reading for the case of 90-degree rotation. Lines 60-63 of

Column 6 describe the address reading for the case of 180-degree rotation. Lines 9-15 of Column 7 describe the address reading for the case of 270-degree rotation).

Regarding **Claim 11**, an image processing method comprising:

an input step of inputting a block image and positional information of the block image (each word or block of image data contains 8 data bits. Refer to Column 4 Lines 6-7 and Line 13. The address generator, Figure 3 Element 19, generates positional information);

an image rotation/reversal processing step of rotating or reversing the input block image by a block, and outputting the rotated or reversed block image (rotation and reversing are performed by Elements 11, 12, 13, and 14 of Figure 3. Refer to Column 4 Lines 52-55); and

a conversion step of converting the positional information of the input block image into the positional information of the image after the rotation or the reversal (conversion is done by reading the proper addresses of image data. The process of rotating an image by 90-degrees is described in Column 6 Lines 5-55. The process of rotating an image by 180-degrees is described in Column 6 Lines 56-68 and Column 7 Lines 1-2. The process of rotating an image by 270-degrees is described in Column 7 Lines 3-33),

wherein the conversion in said conversion step is a process corresponding to the content of the image rotation or the image reversal in said image rotation/reversal processing step, and in the conversion, the positional

information for the entire image before the rotation or the reversal where the block image stands is converted into the positional information for the entire image after the image rotation or the image reversal in said image rotation/reversal processing step, and the converted positional information is added to the rotated or reversed block image and output (refer to Column 6 Lines 49-50, Column 6 Lines 63-65, and Column 7 Lines 9-11).

Regarding **Claim 12**, an image processing apparatus comprising:

input means for inputting a block image and positional information of the block image (each word or block of image data contains 8 data bits. Refer to Column 4 Lines 6-7 and Line 13. The address generator, Figure 3 Element 19, generates positional information);

image rotation/reversal processing means for rotating or reversing the input block image by a block, and outputting the rotated or reversed block image (rotation and reversing are performed by Elements 11, 12, 13, and 14 of Figure 3. Refer to Column 4 Lines 52-55); and

conversion means for converting the positional information of the input block image into the positional information of the image after the rotation or the reversal (conversion is done by reading the proper addresses of image data. The process of rotating an image by 90-degrees is described in Column 6 Lines 5-55. The process of rotating an image by 180-degrees is described in Column 6 Lines 56-68 and Column 7 Lines 1-2. The process of rotating an image by 270-degrees is described in Column 7 Lines 3-33),

wherein the conversion by said conversion means is a process corresponding to the content of the image rotation or the image reversal by said image rotation/reversal processing means, and in the conversion, the positional information for the entire image before the rotation or the reversal where the block image stands is converted into the positional information for the entire image after the image rotation or the image reversal by said image rotation/reversal processing means, and the converted positional information is added to the rotated or reversed block image and output (refer to Column 6 Lines 49-50, Column 6 Lines 63-65, and Column 7 Lines 9-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 9, 10 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,929,085 to Kajihara in view of U.S. Patent No. 5,563,625 to Scott.

Regarding **Claims 9 and 10**, Kajihara discloses an image processing method and apparatus capable of rotating an image by performing bit-order reversing (refer to Figure 3 Elements 11 and 12), and rotating (refer to Figure 3

Elements 13 and 14). A module similar to the numerical signal generation module of sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal is described in Kajihara's invention (Kajihara's method of synchronizing the sequential image data with a pulse is equivalent to having binary signals synchronized with a clock signal. Refer to Column 2 Lines 66-68, and Column 3 Lines 1-3). The bit-order reversing circuit receives image data sequentially, and selectively reversing positions of data bits (refer to Column 1 Lines 66-68, and Column 2 Lines 1-2). The rotation circuit performs image rotation according to instructions from the controller (refer to Figure 3 Element 18, and Column 2 Lines 58-61). The rotating method consists of selectively and sequentially receiving and holding image data in synchronization with a pulse (refer to Column 2 Lines 66-68), and shifting the bits in synchronization with a pulse (refer to Column 3 Lines 1-3). A storage means (Column 4 Lines 6-7) for storing image data. Kajihara also discloses that the buffer memory (refer to Figure 3 Element 15) receives address signals from the address generator (refer to Figure 3 Element 19). Since the input image data is sequentially received, it is clear that all of the image data are one dimensionally arranged. Also, the image data written in memory is read according to addresses of predetermined order so as to perform the rotation process. For the case of 0-degree rotation, the data is read out in a particular way (refer to Column 6 Lines 2-4). For the case of 90-degree rotation, the data is read out in a different way (refer to Column 6 Lines 50-54). Column 6 Lines 60-63 describe how the data is read out for the case of 180-degree rotation. Column 7 Lines 9-15 describe how the data is read out for

the case of 270-degree rotation. Kajihara does not disclose a storage medium which stores a program to control the image processing apparatus.

Scott, on the other hand, discloses an image processing software program, which controls an image processing apparatus (refer to Figure 1 Elements 10 and 11). The software program is capable of performing image rotation and reversal. Although Scott does not describe the storage medium that stores the software (Figure 1 Element 11), it is clear that a software program must be stored in a storage medium.

Therefore, one having ordinary skill in the art can certainly utilize Scott's invention to build a software program, which has features as disclosed in Kajihara's invention (bit reversing module, control module, sequentially reading and outputting data in synchronization with a clock signal, generating address signals, and reading the addresses of the written data in a predetermined order). The motivation to do so is to physically provide a compact and portable design for the image processing system. It is compact and portable because the software program can certainly be stored on a CD-R or a CD-RW, and can be moved around to many different computer systems.

Regarding **Claim 13**, Kajihara discloses an image processing method and apparatus capable of rotating an image. The bit-order reversing circuit (refer to Figure 3 Elements 11 and 12) receives image data in units of words (refer to Column 4 Lines 6-7 and Line 13). So each word is equivalent to a block of 8 data bits. The rotation circuit performs image rotation according to instructions

from the controller (refer to Figure 3 Element 18, and Column 2 Lines 58-61). Kajihara also discloses that the buffer memory (refer to Figure 3 Element 15) receives address signals from the address generator (refer to Figure 3 Element 19); so these address signals are equivalent to the positional information. The positional information (data address) is converted and then outputted (for the case of 90-degree rotation, refer to Figures 8A, 8B, 8C, and 8D for illustration).

Scott discloses an image processing software program, which controls an image processing apparatus (refer to Figure 1 Elements 10 and 11). The software is capable of performing image rotation and reversal. Although Scott does not describe the storage medium that stores the software (Figure 1 Element 11), it is clear that a storage medium must exist to store the software.

Therefore, one having ordinary skill in the art can certainly utilize Scott's invention to build a software program, which has features that include rotation, and conversion modules as disclosed in Kajihara's invention.

Conclusion

Any inquiry concerning this communication or earlier communications should be directed to Jason Vuong at 703-306-4157. The examiner can normally be reached on Monday-Friday from 8:00 A.M. to 5:00 P.M.

KAWilliams

KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER